

Motivation and Approach

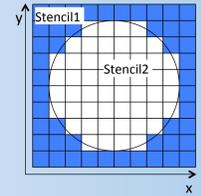
- Accelerate **stencil computation** (nearest neighbors used for computation) algorithms:



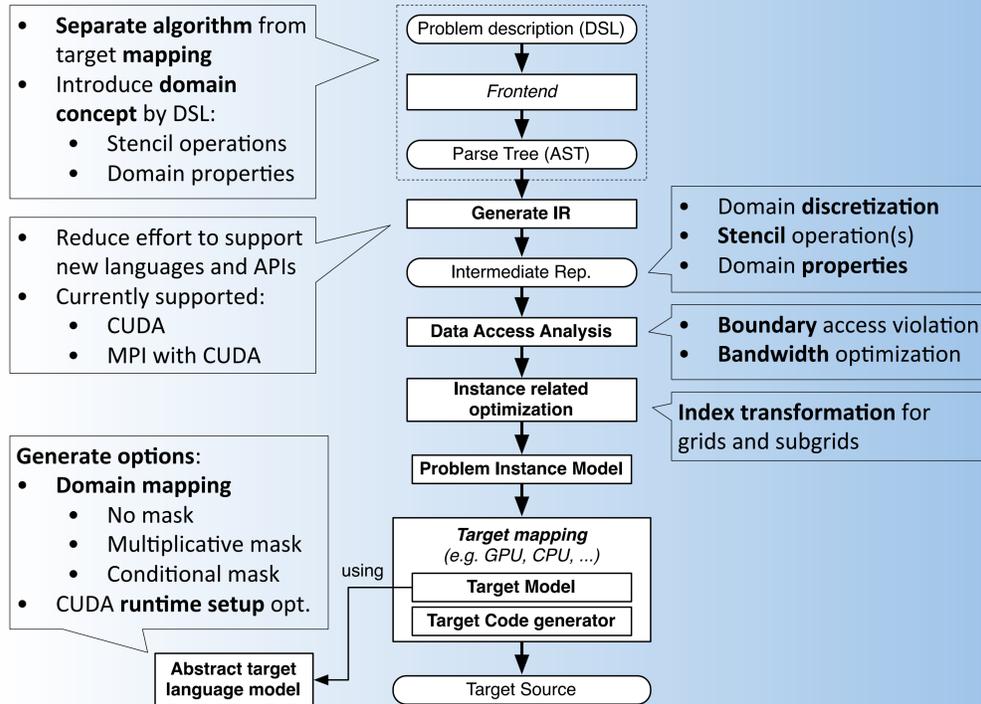
- Algorithms share the property of **regular memory access pattern**
- Allow **transparent usage of accelerators** by domain experts
- Support multiple architectures** e.g.: Multi-Cores, GPUs, FPGAs, ...
- Separating the algorithm description from mapping to hardware architecture** (by high-level language (DSL))
- Introducing the novel **concept of domains and subdomains**
- Efficient code generation** by input and output representation

Domain and Subdomain concept

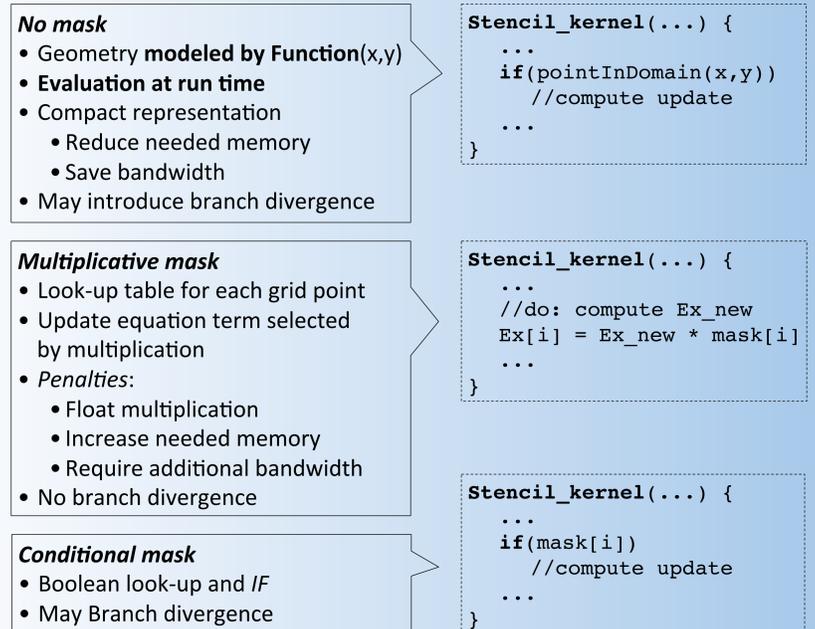
- Real world problems consist of **regions with different properties**
- Discretization** of continuous problem space
- Mapping of regions to domains and subdomains** with arbitrary:
 - Geometry
 - Position in space
 - Operations
 - Properties (e.g. Constants)
- Subdomains** have a **hierarchical relationship** to domains
 - Share properties with parent domain
- Modeling of border properties** by domain concept
- Example:** micro disk cavity in a perfect metallic environment



Code generation tool flow



Domain mapping Optimizations



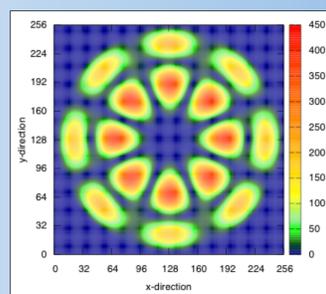
Real-world example

- Realistic **nanophotonic device**
 - Vacuum microdisk** cavity enclosed in a **perfect metallic environment** (two subdomains)
 - Point-like time-dependent inhomogeneity (optical dipole **point source**)
- Using **Maxwell PDEs** to describe evolution of electromagnetic fields
- Numerical approximation by Finite-Difference Time-Domain method (**FDTD**)
- Known **analytic solution** (Whispering Gallery Modes)
- Modeling of different materials by subdomain concept**

$$E_x[i] = ca \cdot E_x[i] + cb \cdot (H_z[i] - H_z[i - dy]) \quad (1)$$

$$E_y[i] = ca \cdot E_y[i] + cb \cdot (H_z[i - dx] - H_z[i]) \quad (2)$$

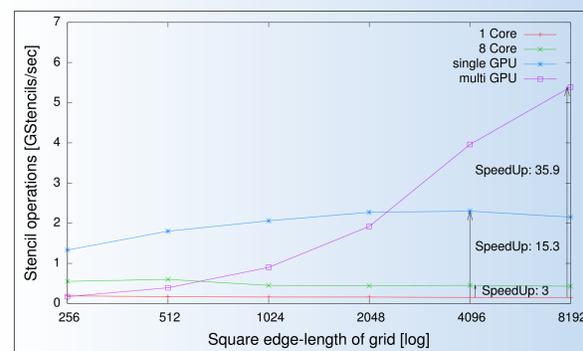
$$H_z[i] = da \cdot H_z[i] + db \cdot (E_x[i + dy] - E_x[i] + E_y[i] - E_y[i + dx]) \quad (3)$$



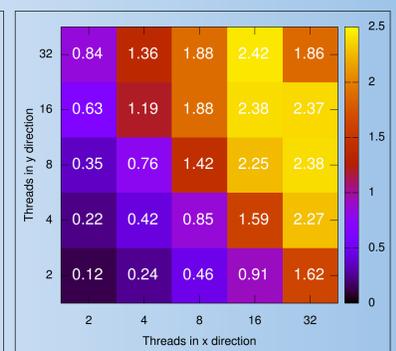
Computed energy density

Results

- Compare reference CPU implementation to:
 - Generated single GPU code (speedup: 15.3x)
 - Generated multi GPU code (speedup: 35.9x)
- Domain mapping options
 - No mask** (2060 MStencils/sec)
 - Multiplicative mask** (2300 MStencils/sec)
 - Conditional mask** (2430 MStencils/sec)



SpeedUP and GStencils/sec over grid size



Runtime setup variation

Outlook / Future Work

- Support more novel hardware architectures
- Optimization strategies for complex memory access pattern

Contact

Björn Meyer
Department of Computer Science
University of Paderborn

E-Mail: bjoern.meyer@uni-paderborn.de
Phone: +49 5251 604343