Woolcano: An Architecture and Tool Flow for Dynamic Instruction Set Extension on Xilinx Virtex-4 FX

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1 Woolcano architecture

Virtex4 FX PowerPC 405 Core

2 Software workflow

application (source code)

policies agreed

intermediate-rep (IR)

LLVM back-end (IR)

problem information

selection of CIs

implementation and configuration

HDL generator pass

communication pass

LLVM passes

3 Case study - software

Toolchain for Dynamic Instruction Set Extension on Xilinx Virtex-4 FX

4 Case study - hardware

5 Results

Architecture Software Floating-point emulation Xilinx APU (EU) Woolcano FCM

cycles 1/2/3/5/7/9 369/183 39/183

openloop vs. emulation 1.00 32.93 39/183

openloop vs. APU (EU) 0.83 1.00 1.21

ICAP initialization Reconfiguration

cycles 1/7/9 179/91/182

6 Contributions

We introduce the Woolcano architecture

- processor with custom instructions
- custom instructions can be changed at runtime
- practically applicable (not simulation)

Compilation toolflow based on LLVM

- automated translation of software to hardware
- generates software binaries with custom instructions

Future work

- automatic custom instruction identification
- improve hardware generation
- from combinational logic to sequential
- this will allow for operators re-use
- develop runtime system that allows for transparent application acceleration with hardware accelerators