**Woolcano: An Architecture and Tool Flow for Dynamic Instruction Set Extension on Xilinx Virtex-4 FX**

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### 1 Woolcano architecture

**Virtex4 FX PowerPC 405 Core**

- GPU pipeline
- Core: tech, config, execution, write back
- Instruction set: 20 registers
- MMU
- DDR-333 SDRAM
- I/F: clock

**Woolcano FCM**

- FCM controller
- I/O bus macro
- Partially reconfigurable region (PFRS) by ICAP (instruction slot)

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### 2 Software workflow

**LLVM pipeline**

- IR
- Optimization
- Configuration
- PCC assembly
- HDL for CI

**HDL pipeline**

- Xilinx Partial Reconfiguration
- Result bus
- BUF macro
- Custom UDI1 instr
- Custom UDI2 instr
- Custom UDI3 instr

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### 3 Case study - software

- HLS
  - Application source code
  - Xilinx bitstream
- Tool: Woolcano
  - Define custom instr
  - Generate bitstream
  - Load custom instr

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### 4 Case study - hardware

- Pipeline stage
  - 2 cycles
  - multiplications
  - add instructions

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### 5 Results

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Software floating-point emulation</th>
<th>Xilinx APU FPU (2:1)</th>
<th>Woolcano FCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>cycles</td>
<td>1,851,623/640</td>
<td>31,752/384</td>
<td>26,307/660</td>
</tr>
</tbody>
</table>

**Instruction throughput**

- Simplex vs. se emulation: 1.00
- Complex vs. APU FPU: 0.03

**ICAP initialization**

- 1812 cycles: 1784.750

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### 6 Contributions

- We introduce the Woolcano architecture
  - Processor with custom instructions
  - Custom instructions can be changed at runtime
  - Practically applicable (not simulation)

**Compilation workflow based on LLVM**

- Automatic translation of code to hardware
- Generates software binaries with custom instructions

**Future work**

- Automatic custom instruction identification
- Improve hardware generation
  - From combinational logic to sequential
  - This will allow for operators re-use
  - Develop runtime system that allows for transparent application acceleration with hardware accelerators