CODING AND SIGNAL PROCESSING FOR A MAGNETO-OPTIC RESONANT BIAS COIL OVERWRITE EXPERIMENT

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ABSTRACT

A magnetooptic direct overwrite experiment using the resonant bias coil technique has been carried out. The technique requires even numbered transitions to be written on even numbered clock cycles and odd numbered transitions to be written on odd numbered clock cycles. This constraint is met by double-spaced run-length-limited (d,k,2) codes where the number of consecutive zeros is even. By exploiting the polarity of the transitions, a detection window that is double the size of the code bit period is possible. This paper describes a detection circuit that achieves the enlarged detection window and presents a phase detector which is particularly simple to implement. Channel bit error rate measurements have been carried out employing a rate 1/3 (2,8,2) code. Error rates of 10^{-8} were achieved for recording densities up to 33 kb/inch. The results further demonstrate the expected excellent immunity of the direct overwrite scheme to bloom.

1. Introduction

Magnetooptic recoding offers the potential of very high areal density erasable data storage. Current recording schemes usually require two revolutions of the disk to overwrite old data with new data: in the first pass the old data is erased by applying an unmodulated writing laser beam and resetting the magnetization to its initial state and in the second pass the new information is written. Recently single-pass ("direct") overwrite schemes have been proposed which utilize time-varying magnetic fields [1 – 3]. In the direct overwrite scheme that uses "field modulation" [1,2] a coil that generates the applied magnetic field is brought in the close vicinity of the disk. The current of the coil and thus the magnetic field is modulated, i.e. is switched rapidly between the two possible orientations according to the binary data pattern to be recorded. The laser heats up an element of the disk such that the magnetization of the element is changed according to the applied field. One disadvantage of the scheme, however, is that high data rate operation requires the coil diameter and the coil-to-media spacing to be small. This limitation is a result of the stored magnetic field energy which must be refreshed each time the field is reversed.

The resonant bias coil overwrite technique largely overcomes this problem and allows high frequency operation with coil-to-media spacing on the order of 1 mm [3]. Here a sinusoidal magnetic bias field is generated by a bias coil which is part of a resonant circuit. Circular magnetic domains of either sign are written by timing the laser pulse to coincide with either positive or negative peaks of the field. Instead of directly modulating the applied magnetic field, the data determines the firing pattern of the laser and through this the orientation of the magnetic domains to be written. If the laser firing rate is sufficiently high, successively written domains will overlap. Variable length domains can be generated by using the overlap of adjacent marks. An important advantage of the resonant bias coil overwrite technique is that the bias field is sinusoidal and independent of the data written. Consequently the technique is compatible with multi-channel recording using laser arrays.

As will be explained in section 2 the resonant bias coil direct overwrite method requires an even number of clock cycles between successive transitions. This can be achieved by the use of double-spaced codes, which are an example of run-length-limited (RLL) codes with multiple spacing, first studied by Funk [4] for application in conventional magnetic recording. Recently, Rugar and Siegel showed that the above "even constraint" is no severe impediment, i.e., the performance of the codes appears to be competitive with more traditional (d,k) codes [5].

The resonant bias coil overwrite technique also has significant impact on the detection circuitry or, more precisely, on the clock synchronization. As will be detailed in section 2 a detection window which is double the size of the clock period is possible and can be actually achieved with the circuit described in section 3. Further, a novel phase detector will be presented which is particularly simple to realize.

In section 4 we describe the overall experimental setup. Pseudorandom data is encoded into a rate 1/3 double-spaced PWM code. The channel consists of a maximum slope detector, phase-locked loop, decoder and codeword synchronization circuitry. The channel bit error rate measurements conducted verify the competitiveness of the resonant bias coil overwrite scheme.

2. Code and Detector Requirements

Figure 1 shows the timing diagram and the resulting mark shapes for the resonant coil direct overwrite technique. The applied magnetic field is sinusoidal. Circular domains of either orientation can be written by pulsing the laser in synchronism with the positive and negative peaks of the field. Since the disk velocity is sufficiently low these domains will overlap and produce the depicted mark shapes. A binary one is represented by a transition in magnetization. A one is formed by shifting the timing of the laser pulse train 180^0 with respect to the phase of the sinusoidal field.

To specify the coding constraints caused by this overwrite technique, first the clock frequency must be defined. It is best chosen to be twice the field frequency f_B

$$1/T_c = 2f_B \qquad (1)$$

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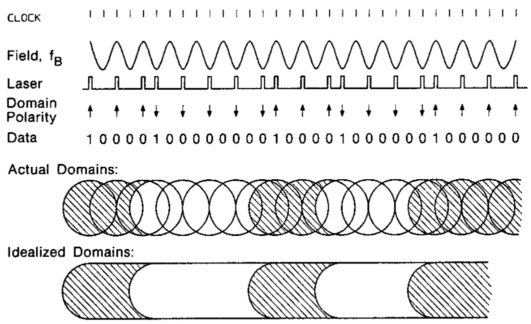

Fig. 1: Timing diagram and resulting mark shapes for the resonant bias coil overwrite technique.

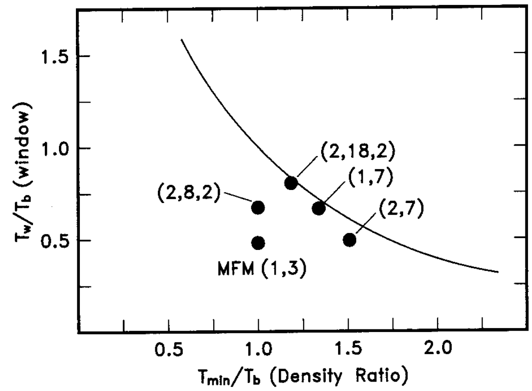

Fig. 2: Operating points of 3 standard and two double-spaced RLL codes.

since the laser can be fired at either the positive or negative excursions of the field. T_c will be called code bit period and clock period interchangeably. Since transitions (binary ones) can only be written when the field has reversed its sign an opportunity for writing a one occurs only every other clock cycle. Therefore the number of consecutive zeros must be even. Special run-length-limited codes that encode arbitrary user data in the data sequence that is actually written on the disk have been designed by Funk [4] and Rugar, Siegel and Weigandt [5,7]. The codes make sure that the number of consecutive zeros is even and also incorporate constraints on the minimum (d) and maximum (k) run-length of zeros. These so-called double-spaced codes are designated (d,k,2) codes.

Clearly, within two code bit periods there is only one legal location for the next "1" (transition) given the location of the last "1", since the number of zeros in between must be even. This can be exploited by increasing the size of the detection window T_w (which is one code bit period for traditional RLL (d,k) codes) to the size of two code bit periods:

$$T_w = 2T_c \tag{2}$$

A "1" received anywhere within this detection window would be assigned to have been received in that single bit period in which the "1" might be legally located.

It is well known [6] that the maximum theoretical code rate C, the so-called capacity, of a binary (d,k) code can be calculated as the base-two logarithm of the largest real root of the equation

$$z^{k+2} - z^{k+1} - z^{k-d+1} + 1 = 0 \tag{3a}$$

for $k < \infty$, and

$$z^{d+1} - z^{d} - 1 = 0 \tag{3b}$$

for $k \to \infty$. Using the result for $k \to \infty$ Funk derived the following equation relating the detection window size T_w/T_b and the minimum period between transitions $T_{\min}/T_b$, both normalized to the duration T_b of one user data bit [4]:

$$1 = 2^{-T_w/T_b} + 2^{-T_{\min}/T_b} \qquad ;(k \to \infty, R = C) \tag{4}$$

This result is exact only for R = C, i.e. if the code rate equals the capacity, but may be used as an approximation for the practically more relevant case of R < C. For a fixed user density it is desirable to design modulation codes that maximize both T_w and $T_{\min}$. The detection window size T_w should be large to achieve maximum immunity to timing jitter. The minimum period between transitions or minimum mark length $T_{\min} = (d+1)T_c = (d+1)RT_b$ should be large in order to minimize intersymbol interference. $T_{\min}/T_b$ is often referred to as density ratio. Figure 2 shows graphically the relationship expressed by eq. (4). Shannon's theory says that no binary coding is possible to the right of the solid curve in Fig. 2 [6]. For the above reasons it is desirable to design codes whose operating points are as close to the curve as possible. The points indicated show three (d,k) codes that are used in magnetic recording and two (d,k,2) codes that are compatible with the resonant bias coil overwrite technique. It can be seen that the additional constraint that the number of successive zeros has to be even is no impediment. It is possible to find (d,k,2) codes with operating points close to the curve in Fig. 2. The rate 2/5 (2,18,2) code, which can be realized with moderate complexity [7], seems to compare well with the widely used (2,7) code. Note that the clocking figure of merit which is a measure for the reliability of the clock recovery is given by the ratio of the maximum period between transitions to the detection window

$$CFM = T_{\max}/T_w = (k+1)T_c/T_w. \tag{5}$$

CFM should be as small as possible. For the (2,7) code we have CFM = 8 and the (2,18,2) code yields 9.5 which is only slightly larger. For a detailed comparison, see Rugar and Siegel [5].

3. Clock Synchronization

The task of the timing recovery is to convert the detected transition to a T_c wide pulse aligned to its T_c-clock leading edge. In this section we describe a synchronizer for the resonant bias coil overwrite experiment which takes advantage of the enlarged detection window.

Because the detection window comprises two code bit periods there are two possible alignments of the window with the code bit pattern, i.e., there are two ways in which two consecutive code bit periods can form the detection window. Further, the detection circuitry must continually realign the detection window as new "1"'s are received (see Fig. 3). Since the number of consecutive zeros is even, even numbered transitions can only be written on even numbered clock cycles and odd numbered transistions can

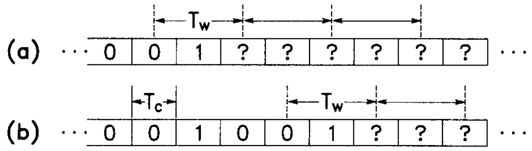

Fig. 3: Continuous realignment of the detection window. In b) a new "1" has been detected and the detection window must be shifted by T_c to obtain the correct alignment for the detection of the next transition.

only be written on odd numbered clock cycles. Therefore with every new "1" received the alignment of the detection window must be changed to the other possible alignment.

If one transition is not detected this results in a permanent dislocation of the detection window and may therefore cause error propagation. If two transitions are not detected the detection window is again correctly aligned. More generally, the detection circuitry must know the number of ones written modulo two for proper alignment.

Funk noticed that this information is just given by the polarity of the transitions [4]. Successive flux transitions alternate in direction and produce readback pulses of alternating polarities. Assume that for a positive polarity pulse the first alignment of the detection window is used and for a negative polarity pulse the second alignment. A positive polarity pulse must follow a negative polarity pulse just as the first alignment of the detection window must follow the second. Exploiting the polarity of the pulses therefore assures proper alignment of the detection window after the occurrence of errors.

The block diagram of Fig. 4 shows the receiver front end and a timing recovery circuit that exploits the two clock period detection window. The readback signal is first passed through a maximum slope detector which consists of a differentiator and a peak detector (National Semiconductor DP8468 [8]). The peak detector was modified slightly to be capable of discriminating peaks of different polarity. A pulse is output on its first output line (ReaD signal Rising edge, RDR) if a peak of positive polarity has been detected. This corresponds to a rising edge at the differentiator input. If a peak of negative polarity has been detected which is caused by a falling edge in the readback signal, a pulse is output on the second output line (ReaD signal Falling edge, RDF). RDR and RDF are the input of the timing recovery circuit. Instead of continuously realigning the detection window we use two phase detectors (PD's). The signal RDR is routed to the first PD, RDF to the second PD. They have identical inner structure (see Fig. 5) but different input signals.

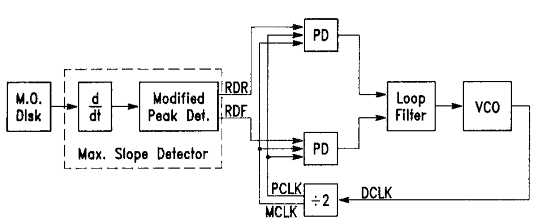

Fig. 4: Block diagram of receiver front end and timing recovery loop.

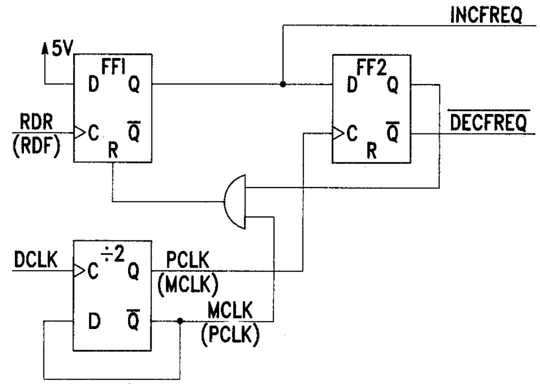

Fig. 5: Phase detector and frequency divider by 2 (lower flipflop). In parenthesis the signal names if PD were used for the second detection window alignment.

The reference signals, against which the phase of the incoming signal is compared are 180° out of phase with periods equal to $T_w = 2T_c$. Therefore the PD's operate on different alignments of the detection window. The error signals generated by the phase detectors are combined and filtered and then drive a voltage controlled oscillator (VCO) which runs at the clock frequency $1/T_c$. To close the feedback loop the frequency of the VCO-output is divided by two and then presented to the input of the phase detectors.

Figure 5 shows that the PD consists of only two flipflops (FF1 and FF2) and an AND-gate. The PD design is based on the one described in [9]. The third FF shown performs the task of frequency dividing the T_c-clock (denoted DCLK) into PCLK and its complement MCLK, whose period is equal to the desired detection window size.

The timing diagram of Fig. 6 illustrates the operation of the PD with RDR at its input. It shows the case of a positive phase error, i.e., the VCO phase lags behinds the phase of the input signal. When a rising edge occurs at the input of the first flipflop (FF1) its Q-output turns to "1". With the next rising edge of PCLK this "1" is transferred to the Q-output of FF2. With the next rising edge of MCLK FF1 is reset and with the next rising edge of PCLK FF2 is reset. Note that the active period of FF1 depends on the phase of the incoming signal and is larger than $2T_c$ for the case shown. The active period of FF2 is independent of the timing of the input RDR and is always $2T_c$ long. The output of the first FF can therefore be used as an "increment frequency" signal and the output of the second FF as a "decrement frequency" signal. Here the INCFREQ signal is active longer than the DECFREQ signal, and therefore the VCO is advanced to catch up with the incoming signal. The two correction signals are displaced in time by T_c seconds, but the high-frequency error signal caused by that is well suppressed by the loop-filter. Therefore the stable lock point of the loop is achieved when the rising edge of the incoming pulse coincides with the falling edge of the reference clock (PCLK for the phase detector illustrated).

The second phase detector operates completely analogously to the first. The only difference is that the input signal is RDF and that PCLK and MCLK are interchanged.

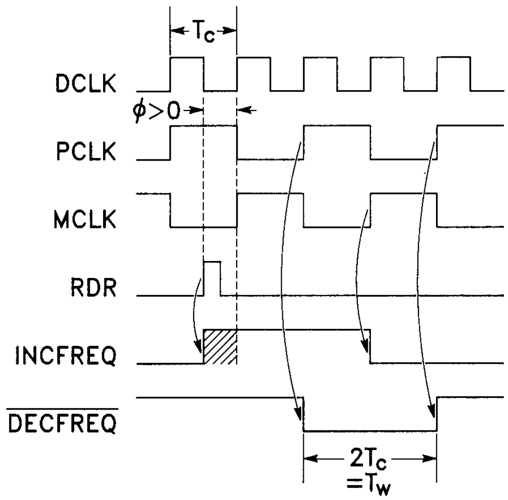

Fig. 6: Timing diagram to explain the operation of the phase detector (positive phase error: $\phi > 0$).

The PD's are not frequency sensitive since it was considered a reasonable assumption that the frequency is quite accurately known a priori and that only phase acquisition in necessary when a new sector of the disk is read. The advantage of the described PD is that no pulses occur that are arbitrarily small for arbitrarily small phase error. Further, compared to other PD for similar applications [8,9] no monostable multivibrator is required.

4. Measurements

To demonstrate and evaluate the resonant bias coil overwrite technique an experimental magnetooptic read/write system was set up. Figure 7 shows its communications block diagram. Pseudorandom data was encoded into Funk's rate 1/3 (2,8,2) PWM code, see Fig. 2 [4]. This code was chosen since the coder and decoder are particularly simple. The implementation of the rate 2/5 (2,18,2) code which achieves 20% larger linear density would have been somewhat more complicated. The code bit patterns were written on a magnetooptic disk with coil spacing approximately 1 mm from the active layer. To write on the disk a Sharp LTO-15 laser was pulsed with 35 ns pulses. The nominal peak write power at the disk was 16.5 mW and the read power 1.5 mW.

The readback signal is first passed through a maximum-slope detector which consists of a differentiator and a modified peak detector which separates the peaks on two output signals according to their polarity. It is followed by the timing recovery, which is described in section 3,

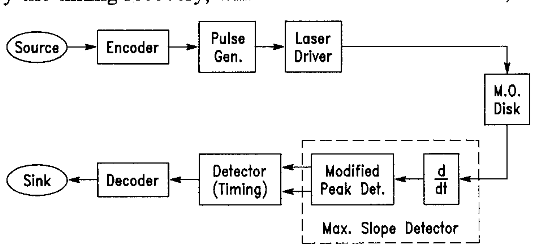

Fig. 7: Communications block diagram of experimental setup.

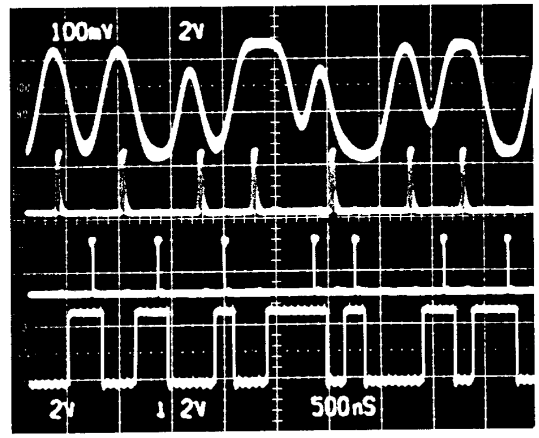

Fig. 8: Sample waveforms (from top to bottom): readback signal; output RDR of peak detector; output RDF of peak detector; NRZ-data.

and the decoder for the (2,8,2) code. In order to correctly recover the user data bits the decoder has the additional task of adjusting the phase of the user data clock (whose frequency is R = 1/3 times the clock frequency $1/T_c$) to match the codeword boundaries. This is done at the beginning of the read process by searching for eight consecutive zeros in the detected code bit sequence. Every run of eight zeroes in Funk's code begins at a codeword boundary. When eight zeroes are detected the data clock phase is adjusted immediately to match the codeword boundaries. No write precompensation or equalization of the readback signal is used. The experiment was carried out with a data rate of 5.3 Mb/s which corresponds to a 16 MHz clock frequency and an 8 MHz coil frequency.

Figure 8 shows a sample readback waveform, the two outputs of the peak detector, and the corresponding NRZ data at the synchronizer output which is aligned with the recovered clock. Note that a peak on the upper pulse train (RDR) corresponds to a local maximum in the slope of the readback signal delayed by approximately 200 ns.

Data patterns were written and the error rates measured at a variety of linear densities by varying the spindle speed. Figure 9 shows that for user data densities below 33 kb/inch the (raw) channel bit error rate was 10^{-8} or below. Precisely, the number 10^{-8} means that no error was detected within 10^9 bits received which was the measurement period.

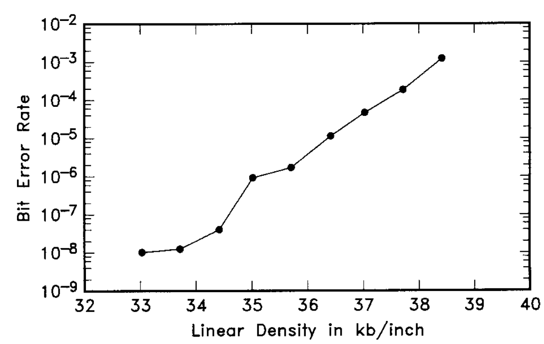

Fig. 9: Channel bit error rate versus linear density in kb/inch.

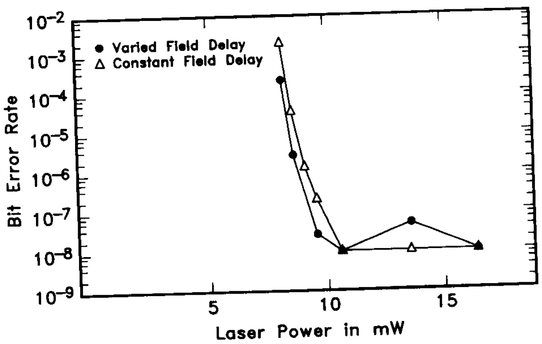

Fig. 10: Channel bit error rate versus writing laser power. "Varied field delay" means that the timing of the laser pulses relative to the sinusoidal field is changed to take into account the dependance of the cooling time of the laser heated spot on the laser power.

Figure 10 presents the channel bit error rate versus write laser power. The error rate remains the same (around 10^{-8}) even when the write laser power is varied by as much as $\pm 20\%$ around its nominal value of 16.5 mW. This shows the excellent immunity of the direct overwrite scheme to bloom, i.e., to variations of the laser power which would cause variations of the size of conventionally written marks. When the write laser power is too low the old data is not erased well enough. This causes the rapid increase in error rate which can be seen in Fig. 10.

5. Conclusions

We have conducted a magnetooptic direct overwrite experiment using a sinusoidal applied magnetic field and a pulsed laser beam. A double-spaced rate 1/3 (2,8,2) run-length-limited code was employed which is compatible with this overwrite technique. Further, a timing recovery cicuit which takes advantage of the double wide detection window is described. It includes a novel phase detector, not limited to this particular application, which is very simple to realize. Channel error rate measurements show that for user densities up to 33 kb/inch the error rate is 10^{-8} or less. The error rate measurements further prove the excellent immunity of the direct overwrite scheme to variations of the laser power.

6. Acknowledgements

The authors gratefully acknowledge useful discussions with P. Siegel, R. Lynch and T. Weigandt, and the assistance of R. Gerber and F. Luecke in setting up the test stand.

7. References

[1] F. Tanaka, S. Tanaka, N. Imamura, *Magneto-optic recording characteristics of TbFeCo media by magnetic field modulation method*, Jpn. J. Appl. Phys., vol. 28, pp. 231-235, Feb. 1987

[2] T. Nakao, M. Ojima, Y. Miyamura, S. Okamine, Y. Takeuchi, Jpn. J. Appl. Phys. 26, Suppl. 26-4, 149 (1987)

[3] D. Rugar, *Magnetooptic direct overwrite using a resonant bias coil*, IEEE Trans. Magn., vol. MAG-24, pp 666-669, Jan. 1988

[4] P. Funk, *Run-length-limited codes with multiple spacing*, IEEE Trans. Magn., vol. MAG-18, pp 772-775, Mar. 1982

[5] D. Rugar, P. Siegel, *Recording results and coding considerations for the resonant bias coil overwrite technique*, Optical Data Storage Topical Meeting, G. R. Knight, C. N. Kurtz (editors), Proc. SPIE 1078, pp 265-270, 1989

[6] C. Shannon, *A mathematical theory of communication*, Bell Sys. Tech. J., vol. 27, pp 393-423 and 623-656, 1948

[7] P. Siegel, T. Weigandt, D. Rugar, unpublished data

[8] National Semiconductor *Mass storage handbook,DP8468 disk pulse detector* and *DP8459 All-code data synchronizer*, March 1988

[9] T. Howell, D. McCown, A. Patel, P. Siegel, *Data detector and clock recovery circuit for dibit (2,8) code*, IBM Techn. Discl. Bull., Vol. 29, No. 2, July 1986