PADERBORN UNIVERSITY

Open Master's Thesis Project

Computer Science Department
Computer Engineering Group
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Implementation of a Performant and Easy-to-use Memory Interface for Recon(R)OS

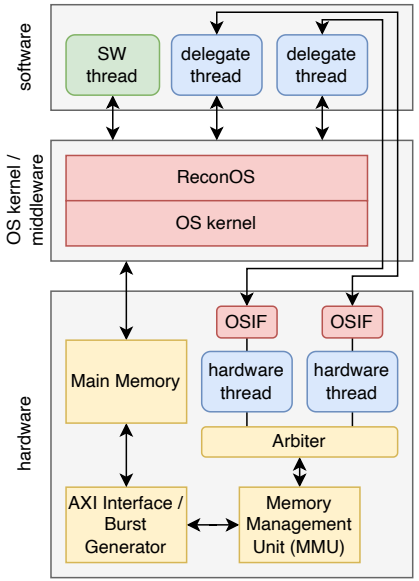
Today, many applications require hardware acceleration to meet their performance requirements. Field Programmable Gate Arrays (FPGAs) are a promising accelerator technology as they can process data highly parallel in an energy-efficient way. Platform FPGAs are systems-on-chip that integrate FPGAs with CPUs. ReconOS is an architecture and programming model for hardware/software multithreading on such platform FPGAs. ReconOS introduces hardware threads that run on the FPGA and interact with the operating system on the CPU in the same way as software threads. ReconROS is an extension of ReconOS for programming robotics applications on platform FPGAs. The ReconOS/ReconROS memory interface allows hardware threads to directly access the main memory. The goal of this thesis is to revise the memory interface for more flexibility in the size of transferred data blocks and for higher performance.

Type of project

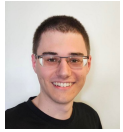
- Design of different approaches and architectures for the memory interface
- Implementation of one of the approaches and a (performance) evaluation of it

Prerequisites

- In-depth knowledge of computer architecture basics
- Basic experience with Linux, HDLs (VHDL or Verilog), and Xilinx tools



ReconOS Architecture



Interested?

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