PADERBORN UNIVERSITY

Computer Science Department
Computer Engineering Group
Prof. Dr. Marco Platzner

Master‘s Thesis

Development of ReconOS/Zephyr on a RISC-V soft CPU

RISC-V is an open instruction set architecture (ISA) that has recently gained more and more popularity. Besides numerous new commercial microcontroller projects also the European Processor Initiative (EPI) relies on this technology. Zephyr is an open-source real-time operating system (RTOS) maintained by the Linux foundation, for which RISC-V support exists. Zephyr comprises a kernel and a set of libraries targeting Internet-of-Things (IoT) applications. The goal of this project is the development of ReconOS/Zephyr running on a RISC-V soft CPU. ReconOS is a reconfigurable hardware operating system enabling hardware/software multithreading on FPGAs. The project starts with the implementation of a RISC-V soft CPU core architecture on a Xilinx FPGA, followed by the adaptation of ReconOS to run under Zephyr. Finally, an evaluation demonstrates the functionality and performance of ReconOS/Zephyr on RISC-V using existing demo applications.

Type of project

- Implementation of a RISC-V soft CPU architecture on FPGA
- Adaptation of ReconOS to the Zephyr RTOS running on RISC-V
- Evaluation of functionality and performance on different demo applications

Prerequisites

- C / C++ / VHDL knowledge

Supervisor

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