PADERBORN UNIVERSITY

Open Master's Thesis Project

Computer Science Department
Computer Engineering Group
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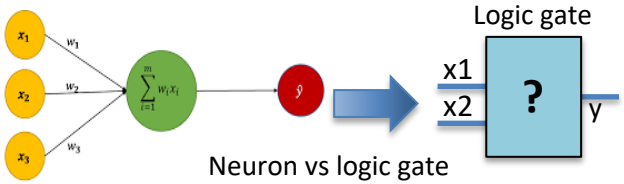
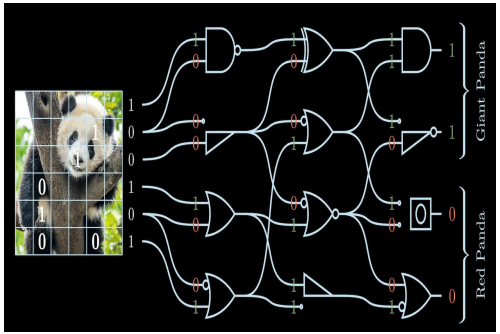
Implementation and Evaluation of Deep Differentiable Logic Gate Networks on FPGA

Deep differentiable logic gate networks are an intriguing new type of deep neural networks (DNN), that were proposed in a recent publication. Logic gate networks implement neurons by simple logic gates such as XOR and AND, and enable fast and efficient inference. Especially extreme-throughput applications can benefit from the approach.

This thesis first focuses on training logic gate networks based on available code and data sets, e.g., MNIST, CIFAR-10. Then, a tool is developed to generate a hardware description from the trained model. Afterward, the logic gate network is synthesized to an FPGA and evaluated. Finally, the resulting accuracy, latency, and hardware cost are compared to other state-of-the-art frameworks for mapping DNNs to FPGAs.



Neuron vs logic gate



Logic gate network

Type of project

- Training and implementing deep differentiable logic gate networks on FPGA
- Evaluating and measuring key hardware related parameters

Prerequisites

- Programing skills, experience with Python/PyTorch, VHDL/Verilog, C/Cuda is a plus
- Basic knowledge of digital circuits, experience with Xilinx FPGAs is a plus

Interested?

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