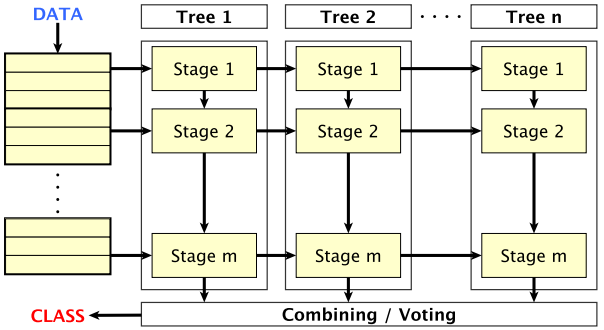
PADERBORN UNIVERSITY

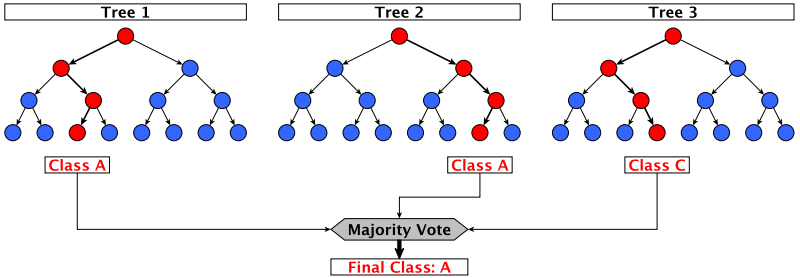
Computer Science Department
Computer Engineering Group
Prof. Dr. Marco Platzner

Master‘s Thesis

Reconfigurable Random Forest Implementation on FPGA



The goal of this thesis is to develop and evaluate different architectures and strategies for implementing Random Forest classifiers on FPGAs. The choice of the architecture affects, for example, the achievable speedup, the potential for partial reprogramming, the area consumption and the reusability of synthesized components.
The result of this work is a system that first trains a random forest for a given dataset and then configures and executes different classifier configurations on a Xilinx Zynq FPGA.



Type of project

- Developing VHDL and/or HLS-code
- Analyze machine learning techniques
- Implementing and evaluating FPGA accelerators

Prerequisites

- C / C++ / VHDL and basic Machine Learning knowledge

Supervisor

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