PADERBORN UNIVERSITY

Open Master's Thesis Project

Computer Science Department
Computer Engineering Group
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Hybrid approximation of DNNs using LogicNets

Deploying Deep Neural Networks (DNNs) on a resource-constrained embedded hardware platform demands a highly optimized representation. Such optimization must be done according to the available hardware resources while maintaining acceptable accuracy. *LogicNet*[1] provides a direct hardware mapping approach for DNNs on LUT-based FPGA aiming for high throughput. While the optimized LUT-based representation is suitable for FPGA-mapping, further LUT-specific optimization that leverages approximate computing can be applied to achieve area savings.

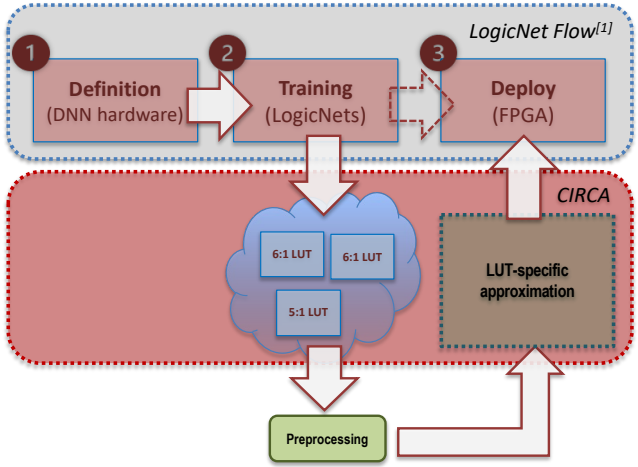
The aim of this thesis is to explore possibilities for approximation of the LogicNets using CIRCA[2] (an open-source framework) as a back-end tool to achieve further area improvements.

Type of project:

1. Preprocessing (including resilience identification) of LogicNet hardware components for use with CIRCA
2. Development of novel LUT-specific approximation technique within CIRCA.
3. Evaluation and comparison of results.

Prerequisites:

Verilog, Python (Experience with PyTorch is plus), basic ML knowledge



[1] Umuroglu, Yaman, et al. "LogicNets: Co-designed neural networks and circuits for extreme-throughput applications." IEEE FPL, 2020. (paper link)

[2] go.upb.de/circa (paper link)

Interested?

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